ABSTRACT OF THE DISCLOSURE

The invention provides a damascene gate process. A semiconductor substrate having a pad layer and an etch stop layer formed thereon is provided, and an insulating layer is formed to cover the etch stop layer, followed by forming an opening by partially removing the insulating layer, the etch stop layer, and the pad layer. A protective spacer is formed on the sidewall of the opening, wherein the top of the protective spacer is lower than the insulating layer. A gate conducting layer is then formed in the opening. The protective spacer and the insulating layer are removed to expose a portion of the semiconductor substrate and the etch stop layer. Implantation is then performed to form lightly doped drains. A gate spacer is then formed to cover the gate conducting layer. The etch stop layer and the pad layer are removed, and implantation is then performed to a form source/drain.